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METHOD AND STRUCTURE FOR IMPROVED MOSFETs USING POLY/SILICIDE GATE HEIGHT CONTROL

Abstract

A method for manufacturing an integrated circuit that has a plurality of semiconductor devices including an n-type field effect transistor and a p-type field effect transistor. This method involves depositing oxide fill on the n-type transistor and the p-type transistor and chemical/mechanical polishing the deposited oxide fill such that a gate stack of the n-type transistor and a gate stack of the p-type transistor, which each have spacers which are surrounded with oxide. The method further involves etching a portion of the polysilicon from a gate of the p-type field effect transistor, depositing a low resistance material (e.g., Co, Ni, Ti, or other similar metals) on the n-type field effect transistor and the p-type field effect transistor, and heating the integrated circuit such that the deposited material reacts with the polysilicon of the n-type transistor and the polysilicon of the p-type transistor to form silicide. The silicide formed on the p-type polysilicon imposes compressive mechanical stresses along the longitudinal di-

rection of the channel of the p-type field effect transistor. A semiconductor device formed by this method has compressive stresses along the length of the PFET channel and tensile stresses along the length of the NFET channel.